

CLAIMS

- 1 1. A process for the fabrication of a semiconductor
2 package, which comprises the following steps:
 - 3 1A) forming wiring on one side of a conductive temporary
4 supporting member;
 - 5 1B) mounting a semiconductor device on said conductive
6 temporary supporting member on which said wiring has been
7 formed, and then electrically connecting a terminal of said
8 semiconductor device with said wiring;
 - 9 1C) sealing said semiconductor device with resin;
 - 10 1D) removing said conductive temporary supporting member
11 to expose said wiring;
 - 12 1E) forming an insulating layer over said exposed wiring
13 pattern at an area other than position where an external
14 connection terminal is to be formed; and
 - 15 1F) forming said external connection terminals on said
16 wiring pattern at said positions where said insulating layer has
17 not been formed.

- 1 2. A process for the fabrication of a semiconductor
2 package, which comprises the following steps:
 - 3 2A) forming wiring on one side of a conductive temporary
4 supporting member;
 - 5 2B) forming an insulating supporting member over said one
6 side of said conductive temporary supporting member, said one
7 side carrying said wiring formed thereon;

8 2C) removing said conductive temporary supporting member
9 to transfer said wiring pattern onto said insulating supporting
10 member;

11 2D) removing said insulating supporting member at
12 positions where an external connection terminal is to be formed
13 for said wiring pattern, whereby a through-holes is formed for
14 said external connection terminal;

15 2E) mounting a semiconductor device on said insulating
16 supporting member on which said wiring has been transferred, and
17 then electrically connecting a terminal of said semiconductor
18 device with said wiring;

19 2F) sealing said semiconductor device with resin; and

20 2G) forming, in said through-hole for said external
21 connecting terminal, said external connection terminal so that
22 said external connection terminal is electrically connected to
23 said wiring.

1 3. A process for the fabrication of a semiconductor
2 package, which comprises the following steps:

3 3A) forming wiring on one side of a conductive temporary
4 supporting member;

5 3B) mounting a semiconductor device on said conductive
6 temporary supporting member on which said wiring has been
7 formed, and then electrically connecting a terminal of said
8 semiconductor device with said wiring;

9 3C) sealing said semiconductor device with resin;

10 3D) removing said conductive temporary supporting member
11 at an area other than position where an external connection
12 terminal for said wiring is to be formed, whereby said external
13 connection terminal made from said conductive temporary
14 supporting member are formed; and

15 3E) forming an insulating layer at said area other than said
16 position of said external connection terminal.

1 4. A process for the fabrication of a semiconductor
2 package, which comprises the following steps:

3 4A) forming an wiring on one side of a conductive temporary
4 supporting member;

5 4B) mounting a semiconductor device on said conductive
6 temporary supporting member on which said wiring has been
7 formed, and then electrically connecting a terminal of said
8 semiconductor device with said wiring;

9 4C) sealing said semiconductor device with resin;

10 4D) forming a metal pattern, which is different in
11 conditions for removal from said conductive temporary supporting
12 member, on another side of said conductive temporary supporting
13 member, said another side being opposite to said one side where
14 said semiconductor device has been mounted, at a position where
15 an external connection terminal for said wiring patterns is to be
16 formed; and

17 4E) removing said conductive temporary supporting member
18 at an area other than said position where said metal pattern has

19 been formed.

1 5. A process for the fabrication of semiconductor packages,
2 which comprises the following steps:

3 5A) forming plural sets of wiring on one side of an
4 insulating supporting member;

5 5B) removing said insulating supporting member at
6 positions where external connection terminals for said wiring
7 are to be formed, whereby through-holes for said external
8 connection terminals are provided;

9 5C) mounting semiconductor devices on said insulating
10 supporting member on which said plural sets of wiring have been
11 formed, and then electrically connecting terminals of said
12 semiconductor devices with said wiring, respectively;

13 5D) sealing said semiconductor devices with resin;

14 5E) forming, in said through-holes for said external
15 connection terminals, said external connection terminals so that
16 said external connection terminals are electrically connected to
17 said wiring; and

18 5F) separating the resultant assembly into individual
19 semiconductor packages.

1 6. A process for the fabrication of semiconductor packages,
2 which comprises the following steps:

3 6A) forming plural sets of wiring on one side of a
4 conductive temporary supporting member;

5 6B) cutting apart said conductive temporary substrate so
6 that said plural sets of wiring formed on said conductive
7 temporary supporting member are divided to include a
8 predetermined number of wiring per unit, and then fixing on a
9 frame said separated conductive temporary supporting member
10 with said wiring formed thereon;

11 6C) mounting semiconductor devices on said conductive
12 temporary substrates on which said wiring have been formed, and
13 then electrically connecting terminals of said semiconductor
14 devices with said wiring, respectively;

15 6D) sealing said semiconductor devices with resin;

16 6E) removing said conductive temporary substrate to expose
17 said wiring;

18 6F) forming an insulating layer over said exposed wiring
19 patterns at areas other than positions where external connection
20 terminals are to be formed;

21 6G) forming said external connection terminals at said
22 positions where said insulating layer for the wiring has not been
23 formed; and

24 6H) separating the resultant assembly into individual
25 semiconductor packages.

1 7. A process for the fabrication of semiconductor packages,
2 which comprises the following steps:

3 7A) forming plural sets of wiring on one side of an
4 insulating supporting member;

5 7B) removing said insulating supporting member at
6 positions where external connection terminals for said wiring are
7 to be formed, whereby through-holes for said external connection
8 terminals are provided;

9 7C) cutting apart said insulating supporting member so that
10 said plural sets of wiring formed on said insulating supporting
11 member are divided to include a predetermined number of wiring
12 per unit, and then fixing on a frame said separated insulating
13 supporting member with said wiring formed thereon;

14 7D) mounting semiconductor devices on said insulating
15 supporting members on which said wiring have been formed, and
16 then electrically connecting terminals of said semiconductor
17 devices with said wiring, respectively;

18 7E) sealing said semiconductor devices with resin;

19 7F) forming, in said through-holes for said external
20 connection terminals, said external connection terminals so that
21 said external connection terminals are electrically connected to
22 said wiring; and

23 7G) separating the resultant assembly into individual
24 semiconductor packages.

1 8. A process for the fabrication of a semiconductor package
2 provided with a single layer of wiring, one side of said wiring
3 having a first connecting function of being connected with a
4 semiconductor device and an opposite side of said wiring having a
5 second connecting function of being to be connected to external

6 wiring, which comprises the following steps 8A, 8B, 8C and 8D:

7 8A) working a heat-resistant insulating base material
8 having a metal foil, thereby forming said metal foil into plural
9 sets of wiring patterns;

10 8B) forming a hole at a position, for exhibiting said second
11 connecting function which is to be formed in a subsequent step,
12 so that said hole extends from a side of said insulating base
13 material to said wiring patterns;

14 8C) bonding a frame base material, which makes an opening
15 through a predetermined portion thereof, to desired position on a
16 surface of said wiring patterns and a surface of said insulating
17 base material, the latter surface being located adjacent to said
18 wiring patterns, respectively; and

19 8D) mounting said semiconductor device, electrically
20 connecting a terminal of said semiconductor device with said
21 wiring pattern, and then sealing said semiconductor device with
22 resin.

1 9. A process for the fabrication of semiconductor packages
2 provided with a single layer of wiring, one side of said wiring
3 having a first connecting function of being connected with a
4 semiconductor device and an opposite side of said wiring having a
5 second connecting function of being connected to external wiring,
6 which comprises the following steps 9A, 9B, 9C and 9D:

7 9A) working a heat-resistant insulating base material
8 having a metal foil, thereby forming said metal foil into plural

9 sets of wiring patterns;

10 9B) forming a hole at a position for exhibiting said second
11 connecting function which is to be formed in a subsequent step,
12 so that said hole extend from a side of said insulating base
13 material to said wiring patterns;

14 9C) bonding a second insulating base material, which makes
15 an opening through a predetermined portion thereof, to a desired
16 position on a surface of said wiring patterns and a surface of said
17 insulating base material, the latter surface being located
18 adjacent to said wiring patterns, respectively, whereby an
19 insulating supporting member is formed;

20 9D) cutting apart said insulating supporting member so that
21 said plural sets of wiring formed on said insulating supporting
22 member are divided to include a predetermined number of wiring
23 per unit, and then fixing on a frame said separated insulating
24 supporting member with said wiring formed thereon; and

25 9E) mounting said semiconductor device, connecting a
26 terminal of said semiconductor device with said wiring, and then
27 sealing said semiconductor device with resin.

1 10. A process for the fabrication of semiconductor
2 packages, which comprises the following steps:

3 10A) forming plural sets of wiring on one side of a
4 supporting member;

5 10B) mounting plural semiconductor devices on said
6 supporting member on which said wiring have been formed, and

7 then electrically connecting terminals of said semiconductor
8 devices with said wiring;

9 10C) subjecting said plural sets of electrically-connected
10 semiconductor device and wiring to gang sealing with resin;

11 10D) removing desired portions of said supporting member
12 to expose predetermined portions of said wiring, and forming
13 external connection terminals so that said external connection
14 terminals are electrically connected to said exposed wiring; and

15 10E) separating the resultant assembly into individual
16 semiconductor packages.

1 11. The fabrication process of semiconductor packages
2 according to any one of claims 1 to 10, wherein subsequent to the
3 sealing of said semiconductor device or devices with said resin, a
4 hardened product of said sealing resin is subjected to heat
5 treatment.

1 12. A semiconductor package fabricated by the process
2 according to any one of claims 1 to 11.

1 13. A process for the fabrication of a semiconductor device
2 packaging frame, said frame being provided with plural
3 semiconductor-device-mounting portions, portions connecting
4 together said plural semiconductor-device-mounting portions, and
5 a registration mark portion, which comprises the following steps:

6 (a) forming wiring for said semiconductor-device-mounting

7 . portions on a conductive temporary substrate,
8 (b) transferring said wiring onto a resin substrate, and
9 (c) etching off said conductive temporary substrate;
10 wherein upon etching off said conductive temporary
11 substrate in step (c), said conductive temporary substrate partly
12 remains to form some of said connecting portions.